EECS 16A Spring 2020 — Designing Information Devices and Systems I — Homework 8

This homework is due March 20, 2020, at 23:59.
Self-grades are due March 23, 2020, at 23:59.

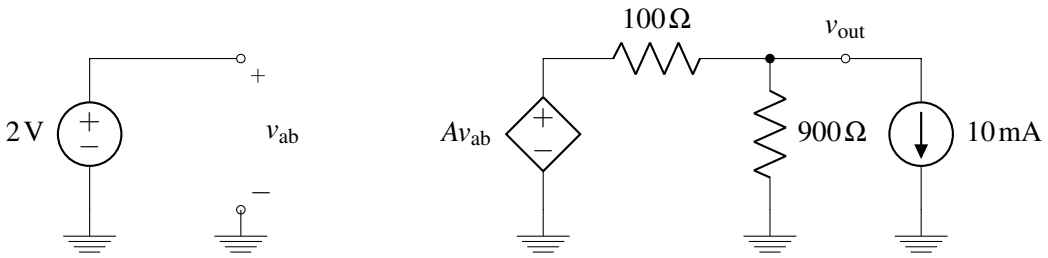
Submission Format
Your homework submission should consist of **one** file.

- `hw8.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. Superposition with a Dependent Source

Given $A = 5$, find the voltage v_{out} indicated in the circuit diagram below using superposition.



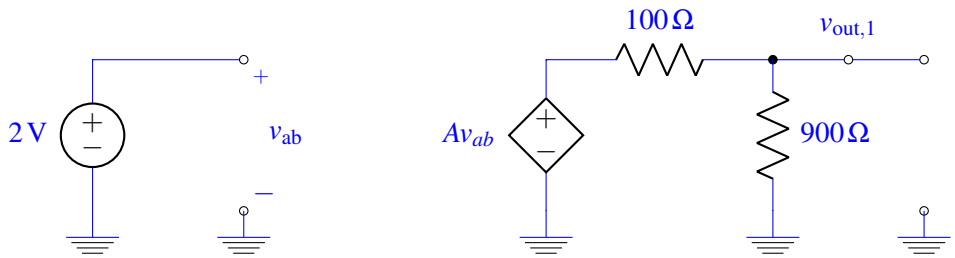
Solution:

$$v_{\text{out}} = 8.1\,\text{V} \tag{1}$$

First, we note that the voltage $v_{ab} = 2\text{V}$ since it is measuring across the voltage source. Our voltage-controlled source will then be $Av_{ab} = 5(2\text{V}) = 10\text{V}$.

Now, consider the circuits obtained by:

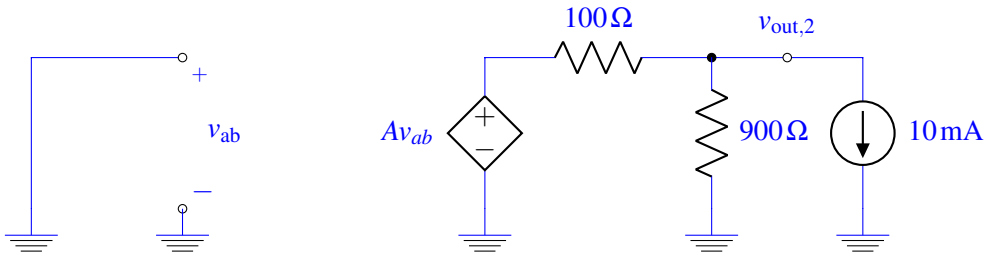
(a) Turning off the current source:



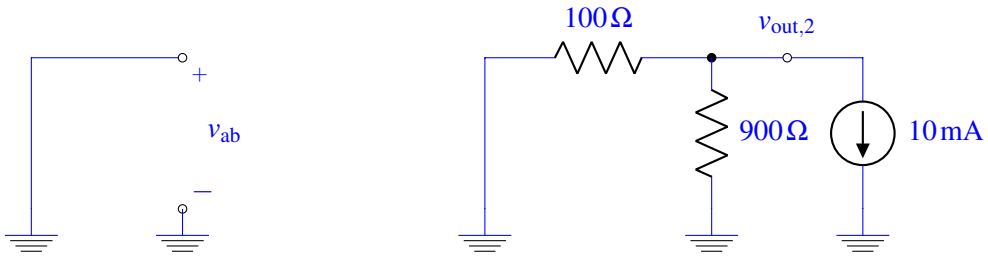
In the above circuit, no current is going to flow through the rightmost branch, as it is an open circuit. Thus this is just a 10 V voltage source connected to a 100 Ω resistor and a 900 Ω resistor in series, so we use the voltage divider formula.

$$v_{\text{out},1} = \frac{900}{100+900}10\,\text{V} = 9\,\text{V}$$

(b) Turning off the voltage source:



Since our independent voltage source is set to zero volts, the voltage V_{ab} will be zero and thus the voltage-controlled source will also be zero. We can redraw the circuit again to reflect this.



Now, looking at the circuit on the right, we have the two resistors in parallel and connected to the current source. The equivalent resistance is given below.

$$R_{eq} = \frac{900(100)}{900+100} = 90\,\Omega \tag{2}$$

Using this equivalent resistance, we find the voltage at $v_{\text{out},2}$ using Ohm's law.

$$v_{\text{out},2} = (-10\,\text{mA})(90\,\Omega) = -0.9\,\text{V} \tag{3}$$

Note that this is a negative voltage since the current is flowing up through the resistors, resulting in a potential at $v_{\text{out},2}$ that is lower than that of the ground node.

Now, applying the principle of superposition, we can solve for v_{out}.

$$v_{\text{out}} = v_{\text{out},1} + v_{\text{out},2} = 9\,\text{V} - 0.9\,\text{V} = 8.1\,\text{V} \tag{4}$$

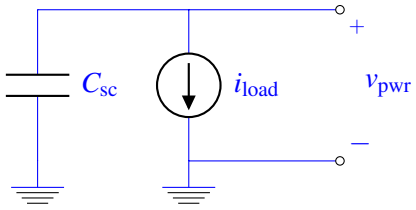
2. Super-Capacitors

In order to enable small devices for the "Internet of Things" (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are "super-capacitors" - the devices generally behave just like a "normal" capacitor but have been engineered to have extremely high values of capacitance relative to other devices

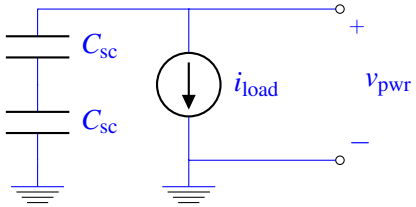
that fit in to the same physical volume. They can function as a power supply for low power applications such as IoT devices and have the advantage that they can be charged and discharged many times without losing maximum charge capacity. That property makes super-capacitors suitable to store energy from intermittent power sources such as those from energy harvesting. Suppose you are tasked with designing a power supply with a super-capacitor in an IoT device.

(a) Assuming that your electronic device (load) can be modeled as a constant current source with a value of i_{load}, draw circuit models for your device using super-capacitors as the power supply with the following configurations:

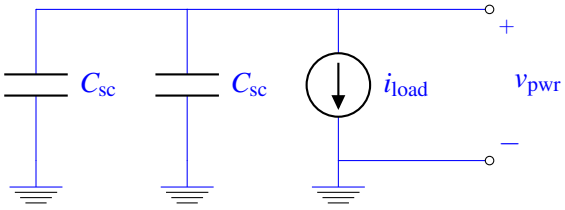
- Config 1: a single super-capacitor as the power supply
  Solution:



- Config 2: two super-capacitors stacked in series as the power supply
  Solution:



- Config 3: two super-capacitors connected in parallel as the power supply
  Solution:



(b) If each super-capacitor is charged to an initial voltage v_{init} and has a capacitance of C_{sc}, for each of the three configurations above, write an expression for the voltage supplied to your electronic device as a function of time after the device has been activated (i.e. connected to the super-capacitor(s)).

Solution:

Let the initial voltage each super capacitor is charged to be v_{init}. We'll now consider the three situations:

- Config 1: **Single super capacitor**
  In this case, the initial voltage that the super capacitor provides is v_{init}, and the initial charge stored in it is then given by $Q_{\text{init}} = v_{\text{init}} C_{\text{sc}}$. Let the voltage at any time, t be defined by $v_{\text{pwr}}(t)$. The charge drained by the constant current source, i_{load} in time t is given by $i_{\text{load}} t$. The effective charge stored

in the capacitor after time t is given by $Q(t) = Q_{\text{init}} - i_{\text{load}}t$. Therefore,

$$\begin{aligned} v_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{sc}}} \\ &= \frac{Q_{\text{init}} - i_{\text{load}}t}{C_{\text{sc}}} \\ &= \frac{v_{\text{init}}C_{\text{sc}} - i_{\text{load}}t}{C_{\text{sc}}} \\ &= v_{\text{init}} - \frac{i_{\text{load}}t}{C_{\text{sc}}} \end{aligned}$$

- Config 2: **Two super capacitors in series**
  In this case, the initial voltage that the effective super capacitor provides is $2v_{\text{init}}$, and the effective capacitance is $C_{\text{eq}} = \frac{C_{\text{sc}}}{2}$. Then, the initial effective charge stored in them is then given by $Q_{\text{init}} = 2v_{\text{init}}C_{\text{eq}} = 2v_{\text{init}}\frac{C_{\text{sc}}}{2} = v_{\text{init}}C_{\text{sc}}$. Let the voltage at any time, t be defined by $v_{\text{pwr}}(t)$. The charge drained by the constant current source in time t is given by $i_{\text{load}}t$. The effective charge stored in the combination after time t is given by $Q(t) = Q_{\text{init}} - i_{\text{load}}t$. Therefore,

$$\begin{aligned} v_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{eq}}} \\ &= \frac{Q_{\text{init}} - i_{\text{load}}t}{C_{\text{eq}}} \\ &= \frac{v_{\text{init}}C_{\text{sc}} - i_{\text{load}}t}{C_{\text{eq}}} \\ &= 2v_{\text{init}} - \frac{2i_{\text{load}}t}{C_{\text{sc}}} \end{aligned}$$

- Config 3: **Two super capacitors in parallel**
  In this case, the initial voltage that the effective super capacitor provides is v_{init}, and the effective capacitance is $C_{\text{eq}} = 2C_{\text{sc}}$. Then, the initial effective charge stored in them is given by $Q_{\text{init}} = v_{\text{init}}C_{\text{eq}} = 2v_{\text{init}}C_{\text{sc}}$. Let the voltage at any time t be defined by $v_{\text{pwr}}(t)$. The charge drained by the constant current source in time t is given by $i_{\text{load}}t$. The effective charge stored in the combination after time t is given by $Q(t) = Q_{\text{init}} - i_{\text{load}}t$. Therefore,

$$\begin{aligned} v_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{eq}}} \\ &= \frac{Q_{\text{init}} - i_{\text{load}}t}{C_{\text{eq}}} \\ &= \frac{2v_{\text{init}}C_{\text{sc}} - i_{\text{load}}t}{C_{\text{eq}}} \\ &= v_{\text{init}} - \frac{i_{\text{load}}t}{2C_{\text{sc}}} \end{aligned}$$

(c) Now let's assume that your electronic device requires some minimum voltage v_{min} in order to function properly. For each of the three super-capacitor configurations, write an expression for the lifetime of the device.

Solution:

The lifetime of a device is the time it takes for the $v_{\text{pwr}}(t)$ to hit the threshold v_{min}. For each of the three configurations, let's find out their lifetime (denoted by t_0):

- Config 1: **Single super capacitor**
  Let us calculate at what time $t = t_0$, $v_{pwr}(t)$ equals v_{min}. We know from the previous part that

$$v_{pwr}(t) = v_{init} - \frac{i_{load}t}{C_{sc}}.$$

  Substituting $v_{pwr}(t) = v_{min}$, we get

$$t_0 = \frac{(v_{init} - v_{min})C_{sc}}{i_{load}}.$$

- Config 2: **Two super capacitors in series**
  Let us calculate at what time $t = t_0$, $v_{pwr}(t)$ equals v_{min}. We know from the previous part that

$$v_{pwr}(t) = 2v_{init} - \frac{2i_{load}t}{C_{sc}}.$$

  Substituting $v_{pwr}(t) = v_{min}$, we get

$$t_0 = \frac{(2v_{init} - v_{min})C_{sc}}{2i_{load}}.$$

- Config 3: **Two super capacitors in parallel**
  Let us calculate at what time $t = t_0$, $v_{pwr}(t)$ equals v_{min}. We know from the previous part that

$$v_{pwr}(t) = v_{init} - \frac{i_{load}t}{2C_{sc}}.$$

  Substituting $v_{pwr}(t) = v_{min}$, we get

$$t_0 = \frac{(v_{init} - v_{min})2C_{sc}}{i_{load}}.$$

Note: We could have also figured it out by finding out how much charge needs to be removed to cause the voltage at the effective capacitance to drop to v_{min}. Thus, we have

$$\Delta Q = (v_{init} - v_{min})C_{eq},$$

which gives us

$$t_0 = \frac{\Delta Q}{i_{load}}.$$

(d) Assume that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor. You consider the two following configurations:

- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel

When is Config 3 (parallel) better than Config 2 (series)? Your answer should involve conditions on v_{init} and v_{min}.

Solution:

It is not obvious from the previous part whether configuration 2 or 3 will provide a longer lifetime. In fact, it depends on what v_{init} is with respect to v_{min}. Let us now see what conditions we need on

v_{init}, such that the parallel configuration provides a longer lifetime, i.e., $t_{0,\text{ parallel}} > t_{0,\text{ series}}$. From the previous part, we get

$$\frac{(v_{\text{init}} - v_{\text{min}})2C_{\text{sc}}}{i_{\text{load}}} > \frac{(2v_{\text{init}} - v_{\text{min}})C_{\text{sc}}}{2i_{\text{load}}}$$
$$2(v_{\text{init}} - v_{\text{min}}) > v_{\text{init}} - \frac{v_{\text{min}}}{2}$$
$$v_{\text{init}} > \frac{3}{2}v_{\text{min}}$$

Thus, we see that when $v_{\text{init}} > \frac{3}{2}v_{\text{min}}$, the parallel configuration is better; otherwise the series configuration is better.

(e) Calculate the amount of energy delivered by the super-capacitors in Config 3 (parallel) over the device's lifetime.

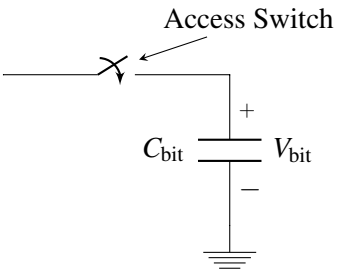
Solution: The initial energy stored by the super-capacitors is $\frac{1}{2}C_{eq}V^2 = C_{sc}v_{init}^2$. At the end of the lifetime, the super-capacitor voltage is v_{min}, so the energy stored in the super-capacitors is $C_{sc}v_{min}^2$. The amount of energy delivered is the difference of the initial and final energies, so it is $C_{sc}(v_{init}^2 - v_{min}^2) = C_{sc}(v_{init} + v_{min})(v_{init} - v_{min})$.

3. Dynamic Random Access Memory (DRAM)

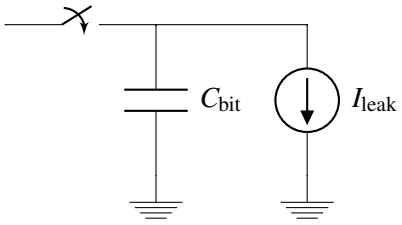
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will model as a leakage to ground. The figure below shows a model of this leakage:



Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

Solution:

We want the time that a cell can read a '1' to be $t_{\text{store}} = 1\,\text{ms}$. We are given that $V_{\text{init}} = 1.2\,\text{V}$ and that $V_{\text{min}} = V_{\text{bit}} = 0.9\,\text{V}$. To get an expression for the leakage rate, we differentiate

$$Q_{\text{bit}} = V_{\text{bit}} C_{\text{bit}},$$

giving

$$I_{\text{leak}} = \frac{dV_{\text{bit}}}{dt} C_{\text{bit}}.$$

Assuming a constant leakage rate, we have

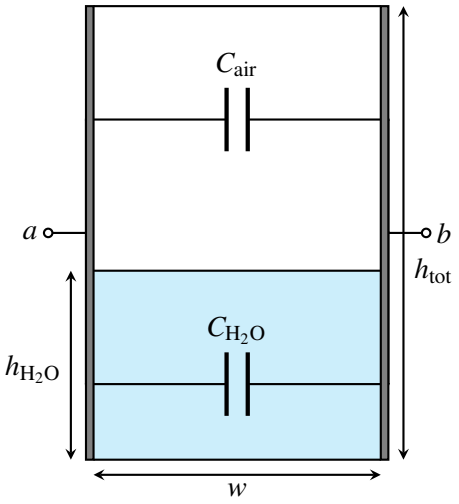
$$\begin{aligned} I_{\text{leak}} &= \frac{\Delta V_{\text{bit}}}{\Delta t} C_{\text{bit}} \\ &= \frac{V_{\text{init}} - V_{\text{min}}}{t_{\text{store}}} C_{\text{bit}}. \end{aligned}$$

Plugging in the values from above, we get

$$\begin{aligned} I_{\text{leak}} &= \frac{(1.2\,\text{V} - 0.9\,\text{V}) \cdot 28\,\text{fF}}{1 \times 10^{-3}\,\text{s}} \\ &= 8.4\,\text{pA}. \end{aligned}$$

4. It's finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com's imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a rectangular tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.



The width and length of the tank are both w (i.e., the base is square) and the height of the tank is h_{tot}.

(a) What is the capacitance between terminals a and b when the tank is full? What about when it is empty? *Note:* the permittivity of air is ε, and the permittivity of rainwater is 81ε.

Solution:

Capacitance of parallel plates is governed by the equation:

$$C = \frac{\varepsilon A}{d},$$

where ε is the *permittivity* of the dielectric material, A is the area of the plates, and d is the distance between the plates. If we apply this to our physical structure, we find that the area of the plates are $h_{tot} \cdot w$, and the distance between the plates is w. The only difference here between a full and empty tank is the permittivity of the material between the two plates.

$$C_{empty} = \frac{\varepsilon_{air} h_{tot} w}{w} = \varepsilon h_{tot}$$

$$C_{full} = \frac{\varepsilon_{H_2O} h_{tot} w}{w} = 81\varepsilon h_{tot}$$

(b) Suppose the height of the water in the tank is h_{H_2O}. Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance C_{tank}.

Solution:

We can break the total capacitance into two parts. First, let's calculate the capacitance of the two plates separated by water:

$$C_{water} = \frac{\varepsilon_{H_2O} h_{H_2O} w}{w} = 81\varepsilon h_{H_2O}$$

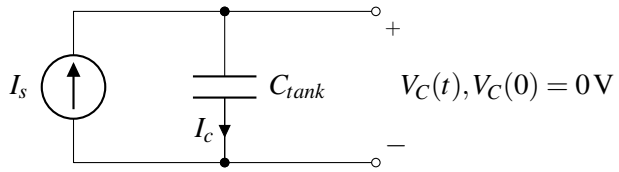
And now we can calculate the capacitance of the two plates separated by air:

$$C_{air} = \frac{\varepsilon_{air} (h_{tot} - h_{H_2O}) w}{w} = \varepsilon (h_{tot} - h_{H_2O})$$

Because these two capacitors appear in parallel, we can simply add our two previous results to find the total equivalent capacitance:

$$C_{tank} = C_{water} + C_{air} = \varepsilon (h_{tot} + 80 h_{H_2O})$$

(c) After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:



In this circuit, C_{tank} is the total tank capacitance that you calculated earlier. I_s is a known current supplied by a current source.

The suggestion is to measure V_C for a brief interval of time, and then use the difference to determine C_{tank}.

Determine $V_C(t)$, where t is the number of seconds elapsed since the start of the measurement. You should assume that before any measurements are taken, the voltage across C_{tank}, i.e. V_C, is initialized to 0 V, i.e. $V_C(0) = 0$.

Solution: The element equation for the capacitor is:

$$I_C = C_{tank}\frac{dV_C}{dt}$$

We also know from KCL that:

$$I_C = I_s$$

Thus, we get the following differential equation for V_C:

$$\frac{dV_C}{dt} = \frac{I_s}{C_{tank}}$$

We recall that I_s and C_{tank} are constant values and the initial value of V_C is zero ($V_C(0) = 0$). Applying these facts and integrating the differential equation, we get the following equation for V_C:

$$V_C(t) = \frac{I_s}{C_{tank}}t$$

(d) Using the equation you derived for $V_C(t)$, describe how you can use this circuit to determine C_{tank} and $h_{\text{H}_2\text{O}}$.

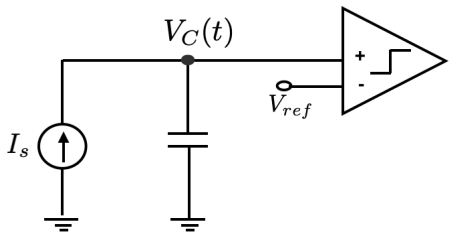
Solution: We connect the current source providing I_s A to the capacitor C_{tank}. At the same time, we can measure $V_C(t)$. After some time passes, we measure $V_C(t)$ and plug it into the following equation (assuming, as before, that $V_C(0) = 0$):

$$C_{tank} = \frac{I_s}{V_C(t)}t$$

If we know C_{tank}, we can determine $h_{\text{H}_2\text{O}}$. Using the equation derived in part (b), we see that

$$h_{\text{H}_2\text{O}} = \frac{C_{tank} - h_{tot}\varepsilon}{80\varepsilon}$$

(e) However, after spending some time thinking about different ways of measuring this capacitance you came up with a better idea. You decided to use the circuit proposed in part (c) along with a comparator, as show in the figure below. What you are basically interested in, is the time T_1 needed for V_c to reach V_{ref}. In order to measure time you use a timer. When voltage V_c becomes larger than V_{ref}, the comparator flips its value and you stop the timer. How would you measure in that case the value of the capacitance?



Solution: We connect the current source providing I_s A to the capacitor C_{tank}. The expression for $V_C(t)$ can be given by:

$$V_C(t) = \frac{I_s}{C_{tank}} t$$

We are interested at measuring T_1 when the V_c reached V_{ref} and the comparator flips. At T_1, V_c is equal to V_{ref}. Therefore by knowing the reference voltage V_{ref} and measuring with a timer T_1, the capacitance can be calculated by:

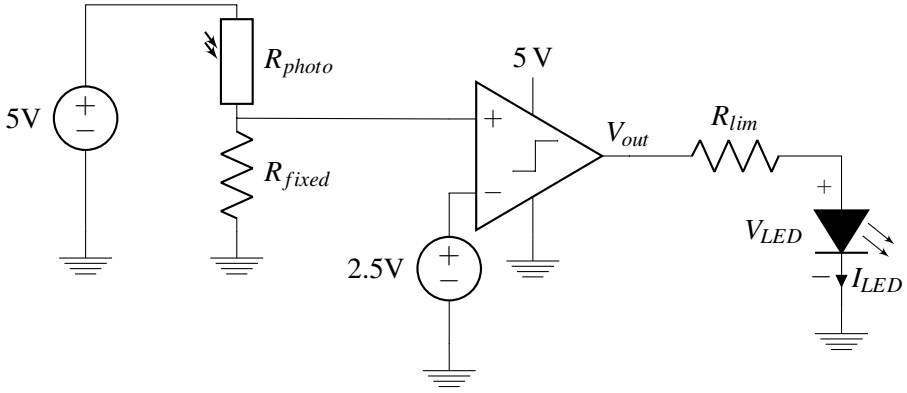
$$C_{tank} = \frac{I_s T_1}{V_{ref}}$$

If we know C_{tank}, we can determine $h_{\mathrm{H_2O}}$. Using the equation derived in part (b), we see that

$$h_{\mathrm{H_2O}} = \frac{C_{tank} - h_{tot}\varepsilon}{80\varepsilon}$$

5. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) "alarm" if the kitchen drawer is opened.



Note R_{photo} is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

V_{LED} indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is V_+, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of R_{photo} and R_{fixed}.

Solution: V_+ is the output of a voltage divider:

$$V_+ = \frac{R_{fixed}}{R_{fixed} + R_{photo}} \cdot 5\,\text{V}$$

(b) We now want to choose a value for R_{fixed}. From the photoresistor's datasheet, we see the resistance in "light" conditions (i.e. drawer open) is $1\,\text{k}\Omega$. In "dark" conditions (i.e. drawer closed), the resistance is $10\,\text{k}\Omega$.

To ensure the comparator detects the light condition with more tolerance, we decide to design R_{fixed} so that V_+ is 3 V under the "light" condition. Solve for the value of R_{fixed} to meet this specification.

Solution: We start from the voltage divider equation we derived in the previous part:

$$V_+ = \frac{R_{fixed}}{R_{fixed} + R_{photo}} \cdot 5\,\text{V}$$

Now we plug in the known values, $V_+ = 3\,\text{V}$ and $R_{photo} = 1\,\text{k}\Omega$.

$$3\,\text{V} = \frac{R_{fixed}}{R_{fixed} + 1000\Omega} \cdot 5\,\text{V}$$

Solving this equation, we get $R_{fixed} = 1.5\,\text{k}\Omega$.

(c) Write down V_{out} with any conditions in terms of V_+. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

Solution:

Since the comparator is ideal, we know that V_{out} will be the voltage at either the positive rail (5 V) or at the negative rail (0 V) when $V_+ \neq V_-$. Which voltage depends on if V_+ is greater than V_- or not. Since V_- is 2.5 V, we get the following piecewise equation for V_{out}:

$$V_{out} = \begin{cases} 5\,\text{V}, & V_+ > 2.5\,\text{V} \\ 0\,\text{V}, & V_+ < 2.5\,\text{V} \end{cases}$$

(d) Using your answers to the previous parts, write down V_{out} with the conditions on its output in terms of R_{photo}. You can substitute the value of R_{fixed} you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

Solution:

We substitute the equations for V_+ into the equation for V_{out}:

$$V_{out} = \begin{cases} 5\,\text{V}, & \frac{R_{fixed}}{R_{fixed}+R_{photo}} \cdot 5\,\text{V} > 2.5\,\text{V} \\ 0\,\text{V}, & \frac{R_{fixed}}{R_{fixed}+R_{photo}} \cdot 5\,\text{V} < 2.5\,\text{V} \end{cases}$$

Plugging in $R_{fixed} = 1.5\,\text{k}\Omega$ from part (b), we can get the following in terms of R_{photo}:

$$V_{out} = \begin{cases} 5\,\text{V}, & R_{photo} < 1.5\,\text{k}\Omega \\ 0\,\text{V}, & R_{photo} > 1.5\,\text{k}\Omega \end{cases}$$

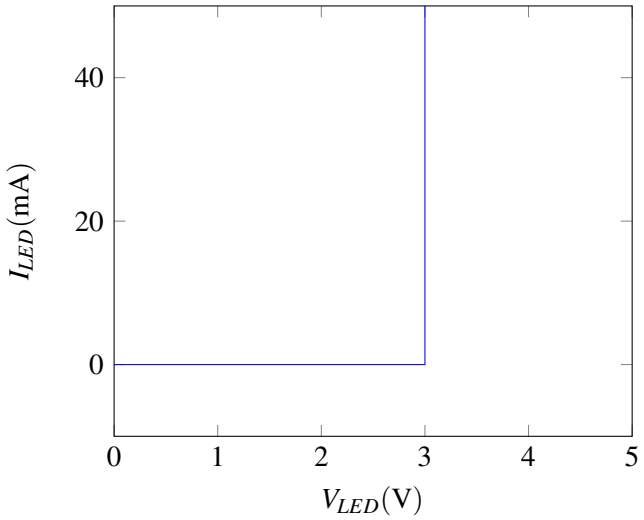
(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED's datasheet, the forward voltage, V_F is 3 V. Essentially, if V_{LED} is less than this voltage, the LED won't light up and I_{LED} will be 0 A.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

i. If the voltage across the LED is less than $V_F = 3\,\text{V}$ or if $I_{LED} < 0\,\text{A}$, then the LED acts like an open circuit.

ii. If the voltage across the LED is $V_F = 3\,\text{V}$, then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).



To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for I_{LED} is 20 mA.

Find the value of the current-limiting resistor, R_{lim}, such that when the photoresistor is in the "light" condition, $I_{LED} = 20\,\text{mA}$.

Solution: When the photoresistor is in the "light" condition, $R_{photo} = 1\,\text{k}\Omega$ so that $V_{out} = 5\,\text{V}$ per the analysis in the previous part. This implies that $V_{LED} = V_F$ and the LED acts like a power supply with positive current flow when in the "light" condition.

Using Ohm's Law and noting that the same current passes through R_{lim} and the LED itself,

$$V_{out} - V_F = I_{LED} R_{lim}$$

Rearranging and plugging in values when in the "light" condition:

$$R_{lim} = \frac{V_{out} - V_F}{I_{LED}}$$

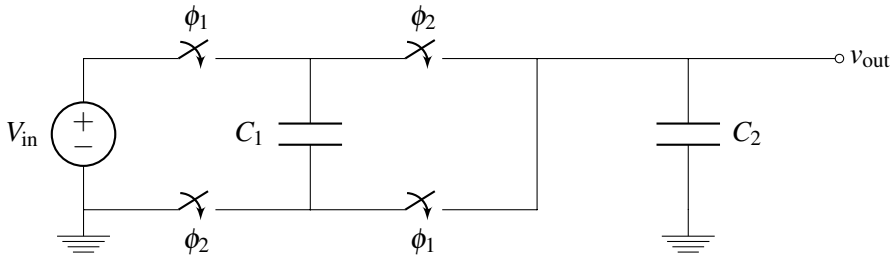
$$R_{lim} = \frac{5 - 3\text{ V}}{0.02\text{ A}}$$

$$R_{lim} = 100\,\Omega$$

Note that when $V_{out} < 3\,\text{V}$, the LED will not light up and I_{LED} will be 0 mA. Thus by our design of the voltage divider, we were able to ensure the LED lights up only if the drawer is opened.

6. DC-DC Voltage Divider

One of the reasons for using AC voltages is that we can easily transform the voltage (step up or step down) using transformers. Unfortunately, such circuits do not work at DC and we need to come up with other ways of dividing DC voltages. We have learned about resistive dividers, but we found inefficiencies. An alternative circuit, a capacitive charge pump, is shown below. It relies on two switches that are activated in sequence. First, switch ϕ_1 is closed (during this period, ϕ_2 switches are open), and then ϕ_2 closes and ϕ_1 is opened. In practice, this is done periodically, but for this problem, we will analyze each phase separately. Note that V_{in} is a DC voltage.



(a) During phase ϕ_1, calculate the voltage across and charge stored by each capacitor C_1 and C_2.

Solution:

Since the two capacitors are connected in series, the same current flows through each one (by KCL), so they both charge to the same value. We can model the system as two capacitors in series, so the amount of charge is given by

$$Q_1 = Q_2 = Q = C_{\text{eq}} V_{\text{in}} = \left(\frac{C_1 C_2}{C_1 + C_2}\right) V_{\text{in}}$$

$$v_1 = \frac{Q_1}{C_1} = \left(\frac{C_2}{C_1 + C_2}\right) V_{\text{in}}$$
$$v_2 = \frac{Q_2}{C_2} = \left(\frac{C_1}{C_1 + C_2}\right) V_{\text{in}}.$$

(b) During phase ϕ_2, calculate the output voltage v_{out} and show that it is a fraction of the input voltage V_{in}.

Solution:

In phase ϕ_2, the two capacitors are in parallel. Note that even if they are charged to different voltages at the end of phase ϕ_1, at the end of phase ϕ_2, their voltages must equalize since they are placed in parallel. In this scenario, similar to putting two batteries in parallel, a large current will flow from one capacitor to the other. Nevertheless, the total charge in the system does not change, so in phase ϕ_2, we

have two capacitors in parallel holding a charge of $Q_{\text{tot}} = Q_1 + Q_2$, and so the output voltage is given by

$$v_{\text{out}} = \frac{Q_{\text{tot}}}{C_1 + C_2} = \frac{2\left(\frac{C_1 C_2}{C_1 + C_2}\right) V_{\text{in}}}{C_1 + C_2}.$$

Simplifying,

$$v_{\text{out}} = \frac{2C_1 C_2}{(C_1 + C_2)^2} V_{\text{in}} < V_{\text{in}}.$$

(c) For the special case of $C_1 = C_2$, calculate the output voltage and the efficiency of the system. To calculate the efficiency, calculate the energy stored in the capacitors at the end of phase ϕ_1 and ϕ_2.

Solution:

For this special case, each capacitor is charged to the same voltage in phase ϕ_1, and so when they are connected in parallel, there is no charge transfer between the capacitors, and the output is exactly half of the input voltage. The derivation above confirms that

$$v_{\text{out}} = \frac{2C^2}{(2C)^2} V_{\text{in}} = \frac{V_{\text{in}}}{2}.$$

The energy stored by C_1 and C_2 at the end of phase ϕ_1 is given by

$$E_{C_1} = E_{C_2} = \frac{1}{2} C \left(\frac{V_{\text{in}}}{2}\right)^2$$

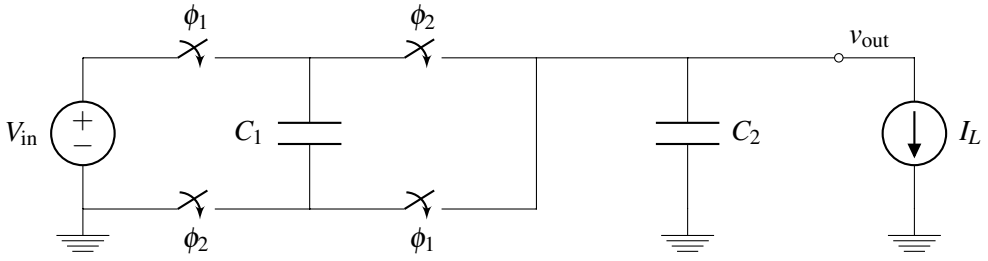
$$E_{\text{tot}_1} = 2 \cdot \frac{1}{2} C \left(\frac{V_{\text{in}}^2}{4}\right) = \frac{1}{4} C V_{\text{in}}^2.$$

At the end of phase ϕ_2, the total energy is stored in two parallel capacitors $C_1 + C_2 = 2C$:

$$E_{\text{tot}_2} = \frac{1}{2}(2C)\left(\frac{V_{\text{in}}}{2}\right)^2 = E_{t,1},$$

which means that no energy is lost in dividing the voltage. If we repeat this calculation in the general case, we will find that unless the division ratio is set at two, there is energy loss. Where does the energy go? In practice, most switches have resistance, and so it goes into heating the switches. What if the switch is ideal? How can you build a circuit that divides by another ratio, say 3, without incurring an efficiency loss?

(d) **PRACTICE:** Assume that this circuit is used with a load represented by the current source $I_L = 10\,\text{mA}$. Suppose that the cycle described above repeats periodically at a rate of 10 kHz, or 10,000 times per second, with each phase ϕ_1 and ϕ_2 lasting exactly 50% of each cycle. During phase ϕ_2, which lasts 50 µs, we want the output voltage to not decrease by more than 5 mV. Specify the capacitances of C_1 and C_2 to satisfy this constraint.



Solution:

During phase ϕ_2, the voltage on the capacitors will decrease due to the load current. For a capacitor, we know that

$$I_C = C\frac{dV}{dt} = (C_1 + C_2)\frac{dV}{dt} = I_L$$

$$\frac{dV}{dt} = \frac{I_L}{C_1 + C_2}.$$

Since the right-hand side is a constant, we have

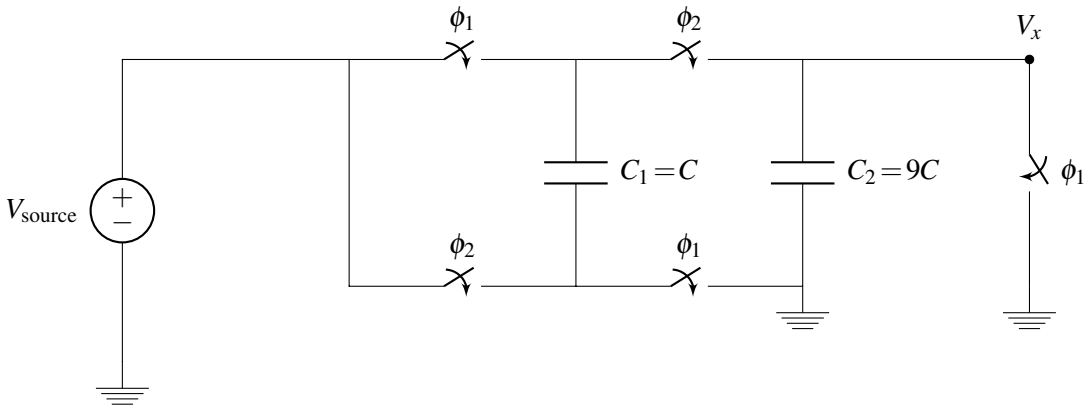
$$\Delta V = \Delta t \frac{I_L}{C_1 + C_2}.$$

Solving for $C_1 + C_2$, we arrive at

$$C_1 + C_2 = \frac{\Delta t I_L}{\Delta V} = 100\,\mu\text{F}.$$

7. (PRACTICE) Charge Sharing

Consider the following circuit:



In the first phase, all of the switches labeled ϕ_1 will be closed and all switches labeled ϕ_2 will be open. In the second phase, all switches labeled ϕ_1 are opened and all switches labeled ϕ_2 are closed.

(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

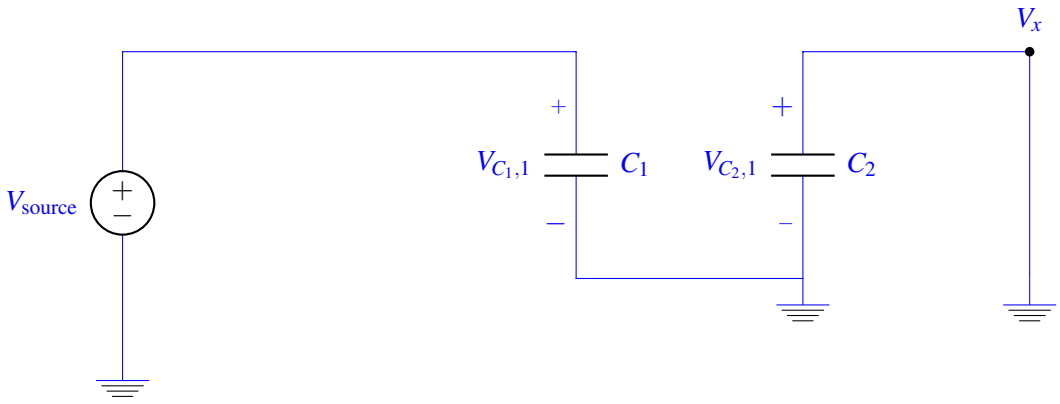
Solution:

One way of marking the polarities is + on the top plate and − on the bottom plate of both C_1 and C_2. Let's call the voltage drop across C_1 V_{C_1} and across C_2 V_{C_2}.

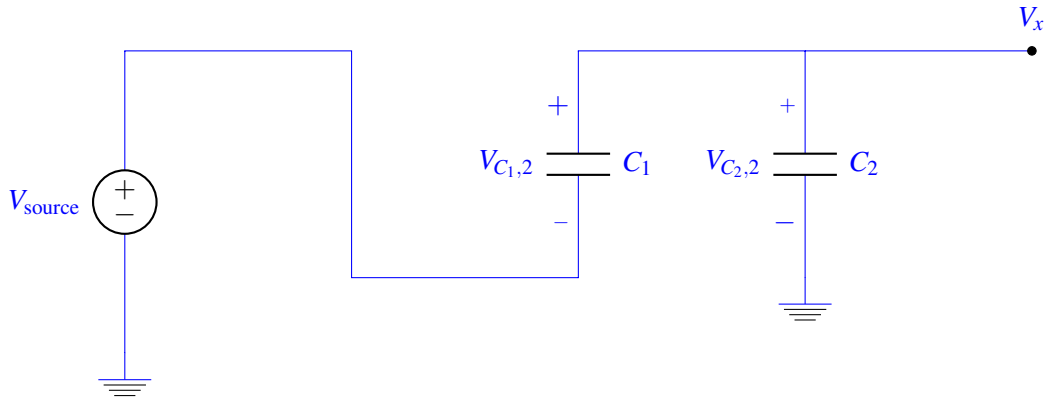
(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

Solution:

Phase 1



Phase 2



In phase 1, all the switches marked as ϕ_1 are closed and switches marked as ϕ_2 are open. In phase 2, all the switches marked as ϕ_2 are closed and switches marked as ϕ_1 are open. Draw both the circuits separately, side by side, with the switches in their respective positions.

(c) Find the voltage across and the charge on C_1 and C_2 in phase 1. Be sure to keep the polarities of the voltages the same!

Solution:

In phase 1,

$$V_{C_1,1} = V_{\text{source}} - 0 = V_{\text{source}}$$

and

$$V_{C_2,1} = 0 - 0 = 0$$

Solution:

Next, we find the charge on each capacitor:

$$Q_{C_1,1} = V_{C_1,1} C_1 = C V_{\text{source}}$$

Note that the positive plate has a charge of $+CV_{\text{source}}$, while the negative plate has a charge of $-CV_{\text{source}}$.

$$Q_{C_2,1} = V_{C_2,1} C_2 = 0$$

(d) Now, in the second phase, find the voltage V_x.

Solution:

Where is charge conserved? To answer this, look at the top plates of C_1 and C_2. In phase 2, they are both "floating" because they are not connected to V_{source} or ground. And in phase 1, they are not connected to each other, but in phase 2, they are connected by the switch. Therefore, in phase 2, the charges on the top plates of C_1 and C_2 will be *shared*, or distributed, because they simply cannot go anywhere else. The total charge will remain the same as in phase 1. Let's find the voltages across C_1 and C_2 in phase 2 (same polarities as in phase 1!):

$$V_{C_1,2} = V_x - V_{\text{source}}$$

and

$$V_{C_2,2} = V_x$$

Now, let's find the charge stored in top plates of C_1 and C_2:

$$Q_{C_1,2} = C(V_x - V_{\text{source}})$$

and

$$Q_{C_2,2} = 9CV_x$$

Next, let's write the equation for charge conservation:

$$Q_{C_1,1} + Q_{C_2,1} = Q_{C_1,2} + Q_{C_2,2},$$

giving

$$CV_{\text{source}} + 0 = C(V_x - V_{\text{source}}) + 9CV_x,$$

which results in

$$V_x = \frac{V_{\text{source}}}{5}.$$

(e) If the capacitor C_2 did not exist (i.e. had a capacitance of 0 F), what would the voltage V_x be?

Solution:

We could always go back to the equations above, plug in $C_2 = 0$, and derive $V_x = 2V_{\text{source}}$. It might be worthwhile to go over what this means for the circuit, though. If $C_2 = 0\,\text{F}$, the capacitor is actually an open circuit. (*Why?*) So we can pretend, as the question says, that C_2 does not exist. In phase 1, as before, C_1 has a voltage drop of V_{source} across it (from top to bottom) and is charged up to CV_{source}. Now, in phase 2, the top plate of C_1 is left dangling (floating). This means that the charge on the top plate of C_1 is going to be the same just like the charge on the bottom plate. We will therefore get

$$V_x = V_{\text{source}} - (-V_{\text{source}}) = 2V_{\text{source}}$$

Recipe for charge sharing:

i. Label all the voltages across the capacitors. Choose whichever direction you want for each capacitor (for example, you can keep the $+$ sign on the top plate and the $-$ sign on the bottom plate of each capacitor, meaning that there is a voltage drop from top to bottom). Just make sure you stay consistent across phases.

ii. Draw the circuit in each phase. Keep the polarities of the voltages across capacitors consistent in all phases!

iii. Look at the circuit in the first phase. First, determine the voltages across each capacitor according to the polarities you have defined. Then, use $Q = CV$ to determine the charge on *each plate of each capacitor*. (Make sure to emphasize the magnitude of charge on each plate. This is important if you want to explain charge sharing conceptually.)

iv. Look at the circuit in the second phase. Determine where the charge is conserved. (Guideline for this: If a plate of a capacitor, or plates of multiple capacitors that are connected to each other in one of the phases, is "floating" in the second phase, meaning that it/they are not connected to any voltage source or ground, then the total charge on the plate(s) must be conserved.)

v. Write the equation for charge conservation. Hence, determine the voltages across the capacitors. Finally, calculate the charge stored in each capacitor in the second phase.

As you probably noticed this exercise was architected in a way that basically walked you through this recipe used to approach charge sharing problems.

8. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?

Solution:

I worked on this homework with...

I first worked by myself for 2 hours, but got stuck on problem 5, so I went to office hours on...

Then I went to homework party for a few hours, where I finished the homework.