This homework is due Friday, July 29, 2022 at 23:59.
Self-grades are due Monday, August 1, 2022 at 23:59.

Submission Format
Your homework submission should consist of one file.

1. Reading Assignment (OPTIONAL)

For this homework, please read Notes 16, 17 and 17B. Note 16 will provide an introduction to capacitors (a circuit element which stores charge), capacitive equivalence, and the underlying physics behind them. Note 17 will provide an overview of the capacitive touch screen, comparator, and Op-Amps. Note 17B will provide a walkthrough of the charge-sharing algorithm.

(a) Describe the key ideas behind how a capacitor works. How are capacitor equivalences calculated? Compare this with how we calculate resistor equivalences.

(b) Consider the capacitive touchscreen. Describe how it works, and compare and contrast it to the resistive touchscreens we have seen in previous lectures and homeworks.

(c) In the charge sharing algorithm, what property of charge is applied in connecting phase 1 calculations to phase 2 calculations?

(d) If the op-amp supply voltages are $V_{DD} = 5\text{V}$ and $V_{SS} = 0\text{V}$, then what is the minimum/maximum value of $V_{out}$?

(e) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touch screen?

Solution:

a) A capacitor is a device that can store charge (and hence, energy) by separating two conducting surfaces with a non-conducting material. This allows equal and opposite amounts of charge to build up on the surfaces, creating a potential difference. Capacitors in parallel can be combined into an equivalent capacitance that is the sum of the individual capacitance (just like resistors in parallel). Capacitors $C_1, C_2$ in series can be combined into an equivalent capacitance of $\frac{C_1 C_2}{C_1 + C_2}$ (just like resistors in parallel).

b) The capacitive touch screen works by detecting a change in capacitance, which is caused by the additional capacitance of a finger being added to the capacitance of the touch screen. The resistive touch screen detects the position of a touch by modeling the touch screen as a voltage divider when pressed down.

c) We apply the conservation of charge at floating nodes to relate measurements in different phases.

a) The minimum op-amp output will always be the value of the $V_{SS}$ supply rail, and thus 0V in this case. The maximum op-amp output will always be the value of the $V_{DD}$ supply rail, and thus 5V in this case.

b) A comparator gives a binary output of either a high value or a low value depending on the difference of voltage between its two input terminals. Thus, comparators can be used as indicators or switches. In the case of a touchscreen, a comparator can indicate whether or not a touch occurs.
This can be done by hooking up one of the comparator terminals to the equivalent capacitance of the touchscreen, and the other terminal to a reference voltage source. The value of this reference voltage source needs to be between the peak of the voltage over the capacitor with and without touch. Thus, when a touch occurs, the difference between the input terminals will invert in sign, and the comparator will respond.

2. It’s finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com’s imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a rectangular tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.

![Diagram of capacitor with plates and dielectric](image)

The width and length of the tank are both \( w \) (i.e., the base is square) and the height of the tank is \( h_{tot} \).

(a) What is the capacitance between terminals \( a \) and \( b \) when the tank is full? What about when it is empty?

*Note:* the permittivity of air is \( \epsilon \), and the permittivity of rainwater is \( 81\epsilon \).

**Solution:**

Capacitance of parallel plates is governed by the equation:

\[
C = \frac{\epsilon A}{d},
\]

where \( \epsilon \) is the *permittivity* of the dielectric material, \( A \) is the area of the plates, and \( d \) is the distance between the plates. If we apply this to our physical structure, we find that the area of the plates are \( h_{tot} \cdot w \), and the distance between the plates is \( w \). The only difference here between a full and empty tank is the permittivity of the material between the two plates.

\[
C_{\text{empty}} = \frac{\epsilon_{\text{air}} h_{tot}w}{w} = \epsilon h_{tot}
\]

\[
C_{\text{full}} = \frac{\epsilon_{\text{H}_2\text{O}} h_{tot}w}{w} = 81\epsilon h_{tot}
\]
(b) Suppose the height of the water in the tank is \( h_{\text{H}_2\text{O}} \). Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance \( C_{\text{tank}} \).

**Solution:**
We can break the total capacitance into two parts. First, let’s calculate the capacitance of the two plates separated by water:

\[
C_{\text{water}} = \frac{\varepsilon_{\text{H}_2\text{O}} h_{\text{H}_2\text{O}} w}{w} = 81 \varepsilon h_{\text{H}_2\text{O}}
\]

And now we can calculate the capacitance of the two plates separated by air:

\[
C_{\text{air}} = \frac{\varepsilon_{\text{air}} (h_{\text{tot}} - h_{\text{H}_2\text{O}}) w}{w} = \varepsilon (h_{\text{tot}} - h_{\text{H}_2\text{O}})
\]

Because these two capacitors appear in parallel, we can simply add our two previous results to find the total equivalent capacitance:

\[
C_{\text{tank}} = C_{\text{water}} + C_{\text{air}} = \varepsilon (h_{\text{tot}} + 80 h_{\text{H}_2\text{O}})
\]

(c) After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:

\[
I_s C_{\text{tank}} \begin{array}{c}
+ \\
V_C(t), V_C(0) = 0 \text{ V}
\end{array} \quad \begin{array}{c}
- \\
I_i
\end{array}
\]

In this circuit, \( C_{\text{tank}} \) is the total tank capacitance that you calculated earlier. \( I_s \) is a known current supplied by a current source.

The suggestion is to measure \( V_C \) for a brief interval of time, and then use the difference to determine \( C_{\text{tank}} \).

Determine \( V_C(t) \), where \( t \) is the number of seconds elapsed since the start of the measurement. You should assume that before any measurements are taken, the voltage across \( C_{\text{tank}} \), i.e. \( V_C \), is initialized to 0 V, i.e. \( V_C(0) = 0 \).

**Solution:** The element equation for the capacitor is:

\[
I_C = C_{\text{tank}} \frac{dV_C}{dt}
\]

We also know from KCL that:

\[
I_C = I_s
\]

Thus, we get the following differential equation for \( V_C \):

\[
\frac{dV_C}{dt} = \frac{I_s}{C_{\text{tank}}}
\]

We recall that \( I_s \) and \( C_{\text{tank}} \) are constant values and the initial value of \( V_C \) is zero (\( V_C(0) = 0 \)). Applying these facts and integrating the differential equation, we get the following equation for \( V_C \):

\[
V_C(t) = \frac{I_s}{C_{\text{tank}}} t
\]
(d) If we can measure $V_C(t)$ and knowing the result of part (c), how could we derive the value of $C_{\text{tank}}$?

Then, using the result from part (b), write $h_{\text{H}_2\text{O}}$ as a function of $C_{\text{tank}}$ and other constants.

**Solution:** We connect the current source providing $I_s$ A to the capacitor $C_{\text{tank}}$. At the same time, we can measure $V_C(t)$. After some time passes, we measure $V_C(t)$ and plug it into the following equation (assuming, as before, that $V_C(0) = 0$):

$$C_{\text{tank}} = \frac{I_s}{V_C(t)} t$$

If we know $C_{\text{tank}}$, we can determine $h_{\text{H}_2\text{O}}$. Using the equation derived in part (b), we see that

$$h_{\text{H}_2\text{O}} = \frac{C_{\text{tank}} - h_{\text{tot}}} {80\varepsilon}$$

3. **Circuit with Capacitors**

Find the voltages at nodes $u_A$ and $u_B$, and currents flowing through all of the capacitors at steady state. Assume that before the voltage source is applied, the capacitors all initially have a charge of 0 Coulombs.

**Solution:** Guide: In general, your strategy to solve circuits with capacitors should be similar to solving resistive circuits. For capacitive circuits we often care about steady state (i.e. what happens to the circuit after a long time and no more changes are happening). If we consider a circuit with capacitors and voltage sources, we will always think about steady state (or the steady state for a phase if we work on a charge sharing problem with switches). When thinking about steady state, you always want to write out the equations for charge that you know, as well as all the KVL type relationships around voltages you know. Then use the key idea that charge is conserved to build out your system of equations. Don’t be daunted by the variable names and know that everything just boils down to a system of linear equations.

Here are some principles that are also helpful:

(a) **Charge at a node from which charge cannot escape or enter (floating node) is always conserved.** — if the sum of charges is 0 on a floating node, the sum of charges on that floating node at steady state will be zero.
(b) The charge \( Q \) stored in a capacitor is given by the equation \( Q = CV \). That is, the plate that corresponds to the "+" terminal, stores \( +Q = +CV \), and the plate that corresponds to the "-" terminal, stores \( -Q = -CV \).

(c) If two capacitors are initially uncharged, and then are connected in series, the charges on both capacitors are equal to each other at steady state.

(d) The voltage across capacitors in parallel is equal at steady state.

**Method 1: Charge conservation**

For a capacitor \( C_k \), let us denote the voltage across it by \( v_{C_k} \), the current flowing through it by \( i_{C_k} \), and its charge by \( Q_{C_k} \). In steady state (that is, after the current has been running for a very long time), direct current (DC) capacitors act as open circuits. Hence, we see that there is no current flowing through the capacitors, that is,

\[
i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0 \text{A}.
\]

To find the voltages across the capacitors, let us label nodes on the circuit as shown in the following figure.

We are going to use the following four properties to find the voltages across the capacitors:

(a) Charge is always conserved at floating nodes.

(b) The charge \( Q \) stored in a capacitor is given by the equation \( Q = CV \).

(c) The charges across series capacitors that are initially uncharged are equal to each other.

(d) The voltage across parallel capacitors is equal.

As an example use of property (c), we have the charge on the capacitor \( C_3 \) equal to the charge on the capacitor \( C_4 \).

Let us start by writing the equation for conservation of charge at node \( u_A \):

\[
Q_{C_1} = Q_{C_2} + Q_{C_3}
\]

By property (b), that is, \( Q = CV \), we can equivalently write this equation for charge conservation in terms of node voltages as

\[
(10V - u_A)3F = (u_A - 0)4F + (u_A - u_B)6F,
\]
which, after simplifying the equation, gives
\[ 30V = 13u_A - 6u_B. \]

Let us then write the charge conservation equation at node \( u_B \); we have
\[ Q_{C_3} = Q_{C_4}. \]

As before, we can write this charge conservation equation in terms of the node voltages as
\[ (u_A - u_B)6F = u_B3F, \]
which, after simplification, gives
\[ 2u_A = 3u_B. \]

Equations 1 and 2 give us two linearly independent equations in two unknowns. Solving the system, we get
\[ u_A = 10/3V, \]
\[ u_B = 20/9V. \]

Using the node voltages, we can calculate the voltages across the capacitors as
\[ v_{C_1} = 10V - u_A = 20/3V, \]
\[ v_{C_2} = u_A = 10/3V, \]
\[ v_{C_3} = u_A - u_B = 10/9V, \]
\[ v_{C_4} = u_B = 20/9V. \]

We write the currents across the capacitors again here for reader’s convenience:
\[ i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0A \]

**Method 2: Capacitor equivalence**

Let’s try to consider another method of solving this. We know that, initially, all the capacitors have charges of 0 C. After a 10 V voltage source is applied, the intermediate node potentials \( u_A \) and \( u_B \) will settle to some steady-state value.

Note that capacitor voltage division only works here because we know the initial conditions of the capacitors before and after the 10 V voltage source is applied. Capacitor voltage division is really just another way of solving for charge redistribution.

Let’s try to find the node potential \( u_A \).
Note that we replaced the capacitors below node $u_A$ with an equivalent capacitance $C_{EQ} = (6\,F \parallel 3\,F) + 4\,F = 6\,F$. The equation for $u_A$ uses the capacitor voltage division formula:

$$u_A = 10\,V \frac{3\,F}{3\,F + 6\,F} = 10/3\,V$$

We can then recognize that the potential $u_B$ is the capacitor voltage division of $u_A$, namely:

$$u_B = \frac{6\,F}{6\,F + 3\,F} u_A$$
$$= \left(\frac{2}{3}\right) 10/3\,V$$
$$= 20/9\,V$$

Note that these are the same values we found using Method 1.

4. Capacitive Touchscreen

The model for a capacitive touchscreen can be seen in Figure 1. See Table 1 for values of the dimensions. The green area represents the contact area of the finger with the top insulator. It has dimensions $w_2 \times d_1$, where $w_2$ is the horizontal width of the finger contact area and $d_1$ is the depth (into the page) of the finger contact area. The top metal (red area) has dimensions $w_1 \times d_1$. The bottom metal (grey area) has dimensions $w \times d_2$, where $w$ is larger than both $w_1$ and $w_2$. The vertical distance between the top metal (red) and bottom plate (grey) is $t_1$, and the vertical distance between the finger (green) and the bottom plate (grey) is $t_2$.

<table>
<thead>
<tr>
<th>$d_1$</th>
<th>10 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d_2$</td>
<td>1 mm</td>
</tr>
<tr>
<td>$t_1$</td>
<td>2 mm</td>
</tr>
<tr>
<td>$t_2$</td>
<td>4 mm</td>
</tr>
<tr>
<td>$w_1$</td>
<td>1 mm</td>
</tr>
<tr>
<td>$w_2$</td>
<td>2 mm</td>
</tr>
</tbody>
</table>

(a) Draw the equivalent circuit of the touchscreen that contains the nodes $F$, $E_1$, and $E_2$ when: (i) there is no finger present; and (ii) when there is a finger present. Express the capacitance values in terms of $C_0$, $C_1$, and $C_2$.

Hint: Note that node $F$ represents the finger. When there is no touch node $F$ would be non-existent. Hint: Treat $E_1$ as the "top node", $E_2$ as the "bottom node", and the finger $F$ as an intermediate node when present.

Solution:
Figure 1: Model of capacitive touchscreen.

Figure 2: Touchscreen circuit with no finger present.
(b) What are the values of $C_0$, $C_1$, and $C_2$? Assume that the insulating material has a permittivity of $\varepsilon = 4.43 \times 10^{-11} F/m$ and that the thickness of the metal layers is small compared to $t_1$ (so you can ignore the thickness of the metal layers). Also assume that the right edge of the top metal (red area) in the diagram is aligned with the right edge of the finger (green area) in the diagram.

**Solution:**

$$C_0 = \varepsilon \frac{d_2 w_1}{t_1} = 2.215 \times 10^{-14} F = 22.15 fF$$

$$C_1 = \varepsilon \frac{d_1 w_1}{t_2 - t_1} = 2.215 \times 10^{-13} F = 221.5 fF$$

$$C_2 = \varepsilon \frac{d_2 (w_2 - w_1)}{t_2} = 1.108 \times 10^{-14} F = 11.08 fF$$

(c) What is the difference in effective capacitance between the two metal plates (nodes $E_1$ and $E_2$) when a finger is present?

**Solution:** The effective capacitance between the two plates is $C_0 = 2.215 \times 10^{-14} F$ when there is no finger. When there is a finger, we have $C_0$ in parallel with a series combination of $C_1$ and $C_2$, giving an additional capacitance $C_1 || C_2 = 1.055 \times 10^{-14} F$ when a finger is present. Therefore, the total effective capacitance is: $3.270 \times 10^{-14} F$.

(d) What are the advantages of capacitive touchscreen over resistive touchscreen?

*Hint: Can we do multi-fingers detections using capacitive touchscreen? What about resistive touchscreen?*

**Solution:** Capacitive touchscreens can implement multi-touch gestures, while resistive screen can only locate a single touch position. In addition, capacitive touchscreens are also highly responsive, as they do not require any pressure to register a touch. Even the slightest touch will activate the screen.

5. Fun With Charge Sharing

(a) Capacitors $C_1$ and $C_2$ are charged to $V_1$ and $V_2$ and switch $S_1$ is open for time $t < 0$. At time $t = 0$, switch $S_1$ is closed. Calculate $V_1$ at time $t > 0$.

Use the following values: $C_1 = 1 F, C_2 = 4 F, V_1 = 6 V, V_2 = 1 V$.

**Solution:**

Let us define the initial charge on $C_1$ as $Q_{i1}$ and the initial charge on $C_2$ as $Q_{i2}$. We know that $Q_{i1} = C_1 V_{i1}$ and $Q_{i2} = C_2 V_{i2}$, where $V_{i1}$ and $V_{i2}$ are the initial voltages across $C_1$ and $C_2$, respectively. (i.e.
Figure 4: Capacitor Charge Sharing

before switch $S_1$ is closed). We know from conservation of charge that $Q_{1i} + Q_{2i} = Q_{1f} + Q_{2f}$, where $Q_{1f}$ and $Q_{2f}$ are the final charge on $C_1$ and $C_2$. (i.e. after switch $S_1$ is closed). We can write this as:

\[ C_1 V_1 + C_2 V_2 = Q_{1f} + Q_{2f} \]

Additionally, we know that once switch $S_1$ is closed, the voltage across $C_1$ and $C_2$ must be the same, because they are now in parallel with each other. Specifically, $V_{1f} = V_{2f}$ where $V_{1f}$ and $V_{2f}$ are the final voltages across $C_1$ and $C_2$, respectively. (i.e. after switch $S_1$ is closed). Therefore,

\[ C_1 V_{1i} + C_2 V_{2i} = (C_1 + C_2)V_{1f} \]

At time $t > 0$, $V_{1f} = V_1 = \frac{C_1 V_{1i} + C_2 V_{2i}}{C_1 + C_2}$

Plugging in numbers, we get:

\[ V_{1f} = 2V \]

(b) The circuit shown below operates in two phases. During phase 1, switches labeled $S_1$ are closed and switches $S_2$ are open. During phase 2, switches $S_1$ are open and switches $S_2$ are closed. Assume that the initial voltage on $C_x = 0$.

i. Redraw the circuit during phase 1. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$. 
ii. Redraw the circuit during phase 2. Replace closed switches with "wires" and open switches with "open circuits" (i.e. just omit them from the diagram). Use $C_1 = C_2 = C_0$.

Solution:

iii. Calculate the value of the voltage $V_{out}$ during phase 2 as a function of $C_0$, $C_x$, and $V_s$. Use $C_1 = C_2 = C_0$.

Solution:  

Step 1: 
Identifying all floating nodes during phase 2. The floating nodes are $V_2$ and $V_x$ since they are connected only to capacitor plates. No current can flow in or out of them.

Step 2: 
For the $V_2$ node:
In phase 1, the total charge is equal to $Q_1 + Q_2 = -C_1V_s + C_2V_s$.
In phase 2, from charge conservation, we get:

$$-C_1V_2 + C_2V_s = C_1V_2 + C_2(V_2 - V_{out})$$  \hspace{1cm} (1)

For the $V_x$ node:
In phase 1, the charge at the bottom plate of $C_2$ was $-C_2V_s$. In phase 2, from charge conservation, we get:

$$-C_2V_s = C_2(V_{out} - V_2) + C_xV_{out}$$  \hspace{1cm} (2)

$$V_2 = \frac{(C_x + C_2)V_{out} + C_2V_s}{C_2}$$  \hspace{1cm} (3)

Plugging (3) into (1),

$$V_{out} = \frac{-C_1C_2V_s}{C_1C_x + C_1C_2 + C_2C_x} = \frac{-V_s}{1 + \frac{C_x}{C_0}}$$
### 6. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) “alarm” if the kitchen drawer is opened.

![Circuit Diagram](attachment:image.png)

Note $R_{\text{photo}}$ is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

$V_{\text{LED}}$ indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is $V_+$, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of $R_{\text{photo}}$ and $R_{\text{fixed}}$.

**Solution:** $V_+$ is the output of a voltage divider:

$$V_+ = \frac{R_{\text{fixed}}}{R_{\text{fixed}} + R_{\text{photo}}} \cdot 5V$$

(b) We now want to choose a value for $R_{\text{fixed}}$. From the photoresistor’s datasheet, we see the resistance in “light” conditions (i.e. drawer open) is 1kΩ. In “dark” conditions (i.e. drawer closed), the resistance is 10kΩ.

To ensure the comparator detects the light condition with more tolerance, we decide to design $R_{\text{fixed}}$ so that $V_+$ is 3V under the “light” condition. Solve for the value of $R_{\text{fixed}}$ to meet this specification.

**Solution:** We start from the voltage divider equation we derived in the previous part:

$$V_+ = \frac{R_{\text{fixed}}}{R_{\text{fixed}} + R_{\text{photo}}} \cdot 5V$$

Now we plug in the known values, $V_+ = 3V$ and $R_{\text{photo}} = 1kΩ$.

$$3V = \frac{R_{\text{fixed}}}{R_{\text{fixed}} + 1000\Omega} \cdot 5V$$

Solving this equation, we get $R_{\text{fixed}} = 1.5kΩ$. 

(c) Write down $V_{out}$ with any conditions in terms of $V_+$. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

**Solution:**

Since the comparator is ideal, we know that $V_{out}$ will be the voltage at either the positive rail (5 V) or at the negative rail (0 V) when $V_+ \neq V_-$. Which voltage depends on if $V_+$ is greater than $V_-$ or not. Since $V_-$ is 2.5 V, we get the following piecewise equation for $V_{out}$:

$$V_{out} = \begin{cases} 
5 \text{V}, & V_+ > 2.5 \text{V} \\
0 \text{V}, & V_+ < 2.5 \text{V}
\end{cases}$$

(d) Using your answers to the previous parts, write down $V_{out}$ with the conditions on its output in terms of $R_{\text{photo}}$. You can substitute the value of $R_{\text{fixed}}$ you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

**Solution:**

We substitute the equations for $V_+$ into the equation for $V_{out}$:

$$V_{out} = \begin{cases} 
5 \text{V}, & \frac{R_{\text{fixed}}}{R_{\text{fixed}} + R_{\text{photo}}} \cdot 5 \text{V} > 2.5 \text{V} \\
0 \text{V}, & \frac{R_{\text{fixed}}}{R_{\text{fixed}} + R_{\text{photo}}} \cdot 5 \text{V} < 2.5 \text{V}
\end{cases}$$

Plugging in $R_{\text{fixed}} = 1.5 \text{k\Omega}$ from part (b), we can get the following in terms of $R_{\text{photo}}$:

$$V_{out} = \begin{cases} 
5 \text{V}, & R_{\text{photo}} < 1.5 \text{k\Omega} \\
0 \text{V}, & R_{\text{photo}} > 1.5 \text{k\Omega}
\end{cases}$$

(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED’s datasheet, the forward voltage, $V_F$ is 3 V. Essentially, if $V_{LED}$ is less than this voltage, the LED won’t light up and $I_{LED}$ will be 0 A.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

i. If the voltage across the LED is less than $V_F = 3$ V or if $I_{LED} < 0$ A, then the LED acts like an open circuit.

ii. If the voltage across the LED is $V_F = 3$ V, then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).
To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for $I_{\text{LED}}$ is 20 mA.

Find the value of the current-limiting resistor, $R_{\text{lim}}$, such that when the photoresistor is in the “light” condition, $I_{\text{LED}} = 20$ mA.

**Solution:** When the photoresistor is in the “light” condition, $R_{\text{photo}} = 1$ kΩ, and based on our analysis in the previous part, $V_{\text{out}} = 5$ V. This implies that $V_{\text{LED}} = V_F$ and the LED acts like a power supply with positive current flow when in the “light” condition.

Using Ohm’s Law and noting that the same current passes through $R_{\text{lim}}$ and the LED itself,

$$V_{\text{out}} - V_F = I_{\text{LED}}R_{\text{lim}}$$

Rearranging and plugging in values when in the “light” condition:

$$R_{\text{lim}} = \frac{V_{\text{out}} - V_F}{I_{\text{LED}}}$$

$$R_{\text{lim}} = \frac{5 - 3 \text{ V}}{0.02 \text{ A}}$$

$$R_{\text{lim}} = 100 \Omega$$

Note that when $V_{\text{out}} < 3$ V, the LED will not light up and $I_{\text{LED}}$ will be 0 mA. Thus by our design of the voltage divider, we were able to ensure the LED lights up only if the drawer is opened.

7. **Op-Amp in Negative Feedback**

In this question, we analyze op-amp circuits that have finite op-amp gain $A$. We replace the op-amp with its circuit model with parameterized gain and observe the gain’s effect on terminal and output voltages as the gain approaches infinity. **Note here that** $V_{SS} = -V_{DD}$. 

For parts (a) - (e) only, assume that the op-amp is ideal (i.e., \( A \to \infty \)). We will consider the case of finite gain \( A \) in parts (f) - (h).

(a) Consider the circuit shown above and \( V_{SS} = -V_{DD} \). What is \( u_+ - u_- \)?

**Solution:** For ideal op-amp circuits in negative feedback, the voltage at the two terminals must be equal, so \( u_+ - u_- = 0 \).

(b) Find \( v_x \) as a function of \( v_{out} \).

**Solution:** We see that \( v_x \) is the middle node of a voltage divider, so \( v_x = v_{out} \frac{R_2}{R_1 + R_2} \).

(c) What is \( I_{R_2} \), i.e. the current flowing through \( R_2 \) as a function of \( v_s \)? *Hint: Find the current through \( R_1 \) first.*

**Solution:** We know from part (a) that \( v_x = v_s \). The current flowing through \( R_1 \) is \( I_{R_1} = \frac{v_s}{R_1} \). This current also flows through \( R_2 \).

(d) Find \( v_{out} \) as a function of \( v_s \).

**Solution:** Using the answer from the previous part, \( v_{out} = v_s + R_2 I_{R_1} = v_s + R_2 \frac{v_x}{R_1} = v_s \left( \frac{R_1 + R_2}{R_1} \right) \).

(e) What is the current \( i_L \) through the load resistor \( R \)? Give your answer in terms of \( v_{out} \).

**Solution:** The current \( i_L \) through the load is \( \frac{v_{out}}{R} \).
(f) We will now examine what happens when $A$ is not $\infty$. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.

Now, using this setup, calculate $v_{out}$ and $v_x$ in terms of $A$, $v_s$, $R_1$, $R_2$ and $R$. Is the magnitude of $v_x$ larger or smaller than the magnitude of $v_s$? Do these values depend on $R$? Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.

Solution:

This is the equivalent circuit of the op-amp:

Since $v_{out}$ is connected to the output of the op-amp, which is a voltage source, we can determine $v_{out}$:

$$v_{out} = A(u_+ - u_-)$$
$$= A(v_s - v_x)$$
Since there is no current flowing into the op-amp input terminals from nodes \( u_+ \) and \( u_- \), \( R_1 \) and \( R_2 \) form a voltage divider and \( v_x = v_{out} \left( \frac{R_1}{R_1+R_2} \right) \). Thus, substituting and solving for \( v_{out} \):

\[
\begin{align*}
  v_{out} &= A \left( v_x - v_{out} \frac{R_1}{R_1+R_2} \right) \\
  v_{out} &= v_x \left( \frac{1}{\frac{R_1}{R_1+R_2} + \frac{1}{A}} \right)
\end{align*}
\]

Knowing \( v_{out} \), we can find \( v_x \):

\[
v_x = \frac{v_x}{1 + \frac{R_2}{AR_1}}
\]

Notice that \( v_x \) is slightly smaller than \( v_s \), meaning that in equilibrium in the non-ideal case, \( v_+ \) and \( v_- \) are not equal. \( v_{out} \) and \( v_x \) do not depend on \( R \), which means that we can treat \( v_{out} \) as a voltage source that supplies a constant voltage independent of the load \( R \).

(g) Using your solution to the previous part, calculate the limits of \( v_{out} \) and \( v_x \) as \( A \to \infty \). You should get the same answer as in part (d) for \( v_{out} \).

**Solution:**

As \( A \to \infty \), the fraction \( \frac{1}{A} \to 0 \), so

\[
v_{out} = v_x \left( \frac{1}{\frac{R_1}{R_1+R_2} + \frac{1}{A}} \right)
\]

converges to

\[
v_x \left( \frac{1}{\frac{R_1}{R_1+R_2} + 0} \right) = v_x \left( \frac{R_1 + R_2}{R_1} \right).
\]

Therefore, the limits as \( A \to \infty \) are:

\[
\begin{align*}
  v_{out} &\to v_s \left( \frac{R_1 + R_2}{R_1} \right) \\
  v_x &\to v_s
\end{align*}
\]

If we observe the op-amp is in negative feedback, we can apply the fact that \( u_+ = u_- \). We get \( v_x = v_s \). Then the current \( i \) flowing through \( R_1 \) to ground is \( \frac{v_x}{R_1} \). By KCL, this same current flows through \( R_2 \) since no current flows into the negative input terminal of the op-amp (\( u_- \)). Thus, the voltage drop across \( R_2 \) is \( v_{out} - v_x = i \cdot R_2 = v_s \left( \frac{R_2}{R_1} \right) \). Therefore, \( v_{out} = v_s + v_s \left( \frac{R_2}{R_1} \right) = v_s \left( \frac{R_1 + R_2}{R_1} \right) \). The answers are the same if you take the limit as \( A \to \infty \).

(h) **[OPTIONAL, CHALLENGE]** Now you want to make a non-inverting amplifier circuit whose gain is nominally \( G_{nom} = \frac{v_{out}}{v_s} = 1 + \frac{R_2}{R_1} = 4 \). However, \( G_{nom} \) can only be achieved only if the op-amp is ideal, i.e., if its internal gain \( A \to \infty \). But, as with most considerations in the physical world, we must account for nonidealities! In reality, because you will be working with an op-amp with finite gain \( A \), your designed circuit gain may come close to but will never quite reach \( G_{nom} \) as a result of the real op-amp’s finite internal gain \( A \).

Suppose you would like your real op-amp circuit to have a maximum error of 1% (i.e., a minimum circuit gain of 3.96, i.e., \( \frac{v_{out}}{v_s} \geq 3.96 \)). Remember that only if your op-amp were ideal, you would have a nominal circuit gain of \( G_{nom} = \frac{v_{out}}{v_s} = 1 + \frac{R_2}{R_1} = 4 \).
What is the minimum required value of $A$, called $A_{\text{min}}$, to achieve that specification? *Hint: Use your expression of $v_{\text{out}}$ in part (f) to find an expression for $G_{\text{min}} = \frac{v_{\text{out}}}{v_s}$ when $A \neq \infty$.*

**Solution:** From the previous part, $v_{\text{out}} = v_s \left( \frac{1}{R_1 R_2 + \frac{1}{A}} \right)$. After algebraic manipulations, we get

$$v_{\text{out}} = v_s \left( \frac{A(R_1 + R_2)}{R_1 + R_2 + AR_1} \right)$$

We are interested in the op-amp’s minimum gain $A_{\text{min}}$, which gives us the circuit’s corresponding minimum gain $G_{\text{min}}$.

We define the minimum (actual - i.e. corresponding to a non-infinite $A = A_{\text{min}}$) gain as: $G_{\text{min}} = \frac{v_{\text{out}}}{v_s}$.

We also define the nominal (ideal - i.e. corresponding to an infinite $A$) gain as: $G_{\text{nom}} = 1 + \frac{R_2}{R_1}$.

Rewriting $A_{\text{min}}$ in terms of $G_{\text{nom}}$ and $G_{\text{min}}$ gives:

$$A_{\text{min}} = \frac{G_{\text{min}} G_{\text{nom}}}{G_{\text{nom}} - G_{\text{min}}}$$

$$= 396$$

Notice that the op-amp’s minimum gain is independent of the resistor values. In general, if we wanted an error of less than $\varepsilon$, then the following will approximately hold: $\frac{A_{\text{min}}}{G_{\text{nom}}} > \frac{1}{\varepsilon}$.

8. **Op Amp Nodal Analysis**

Consider this op amp circuit below. We are interested in analyzing its input-output relationship, finding the Thevenin equivalent of this op amp circuit, and making some observations about the resulting equivalent.

(a) What is the node voltage at $u_1$?

**Solution:** At node $u_1$, if we apply the ideal op amp assumptions, there should be no current going into the positive terminal. This means we can interpret the resistor network attached to the positive terminal as a voltage divider.

$$u_1 = \frac{R}{R + R} V_2 = \frac{V_2}{2}$$
(b) Write a KCL equation at node $u_2$.

**Solution:** At node $u_2$, we can write the KCL equation considering that there will be no current going into the negative terminal.

$$\frac{u_2 - V_1}{R} + \frac{u_2 - u_3}{R} = 0$$

(c) Write a KCL equation at node $u_3$.

**Solution:** At node $u_3$, the KCL equation is:

$$\frac{u_3 - u_2}{R} + \frac{u_3 - 0V}{R} + \frac{u_3 - u_5}{R} = 0$$

(d) Write an expression relating voltages $u_4$ and $u_5$.

**Solution:** At node $u_5$, there is a voltage divider, where $u_4$ is the node voltage that has the same value as the branch voltage of the resistor that bridges terminals $a$ and $b$.

$$u_4 = \frac{R}{R+R} u_5 = \frac{u_5}{2}$$

Note that the output node with node voltage $u_5$ did not have a KCL equation written for it. This is because the output is determined by a dependent voltage source and the current coming out from the source will not be expressible until we’ve found all the node voltages.

(e) Noting that this circuit is in negative feedback and putting together every expression we have derived in previous parts, find an expression for $V_{out}$ as a function of $V_1$ and $V_2$.

**Solution:** Since the circuit is in negative feedback, the input terminal voltages should be the same: $u_1 = u_2$. Substituting into the KCL equations, we have:

$$\frac{u_1 - V_1}{R} + \frac{u_1 - u_3}{R} = 0$$

$$\frac{u_3 - u_1}{R} + \frac{u_3}{R} + \frac{u_3 - u_5}{R} = 0$$

Treating $u_1$ and $V_1$ as knowns, the first KCL equation tells us that $u_3$ is:

$$u_3 = 2u_1 - V_1 = V_2 - V_1$$

Treating $u_3$ and $u_1$ as knowns, the second KCL equation tells us that $u_5$ is:

$$u_5 = 3u_3 - u_1$$

$$= 3V_2 - 3V_1 - \frac{V_2}{2} = \frac{5}{2}V_2 - 3V_1$$

Lastly, our output voltage $u_4 = V_{out} = V_{Th}$ is:

$$u_4 = V_{out} = \frac{\frac{5}{2}V_2 - 3V_1}{2} = \frac{5}{4}V_2 - \frac{3}{2}V_1$$
(f) Turn off all independent sources \((V_1 = V_2 = 0V)\). What is the equivalent resistance as seen between terminals \(a\) and \(b\)? This will be your Thevenin resistance, \(R_T\). (Hint: Consider what the voltage at the output of the op amp becomes and use a test source, or replace the op amp with its internal model where it has a dependent source.)

**Solution:** When both inputs \(V_1\) and \(V_2\) are off, the analysis in the previous subpart showed that \(u_5\), the node voltage at the output of the op amp would be 0V. If this is the case, by applying a test source we have:

\[
0V \quad R \quad I_{\text{test}} \quad V_{\text{test}}
\]

Since both resistors will have branch voltages of \(V_{\text{test}}\) over them, \(I_{\text{test}}\) can be written as:

\[
I_{\text{test}} = \frac{V_{\text{test}}}{R} + \frac{V_{\text{test}}}{R} = \frac{2V_{\text{test}}}{R}
\]

So the equivalent resistance as seen from the output (which is also the Thevenin resistance since we turned off all sources) is:

\[
R_{eq} = \frac{V_{\text{test}}}{I_{\text{test}}} = \frac{R}{2}
\]

Another way to approach the problem is to consider the internal model of the op amp:

\[
\cdots \quad u_5 \quad R \quad + \quad \quad V_{\text{out}} \quad - \\
A(V_+ - V_-)
\]

The output \(u_5\) being zero when \(V_1\) and \(V_2\) are zero essentially means the dependent source is off and behaves like a short - we can turn off the dependent source in this case because it is directly influenced by the independent sources \(V_1\) and \(V_2\):

\[
\cdots \quad R \quad + \quad V_{\text{out}} \quad -
\]

In this scenario, the equivalent resistance seen at the output is just \(R||R = \frac{R}{2}\) since the resistors are in parallel.

(g) Use what you found in previous parts to draw the Thevenin equivalent.

**Solution:** The Thevenin equivalent is given by the following circuit:
(h) **Practice (Optional):** Does the Thevenin resistance depend on all the resistors or a strict subset? What might explain this?

**Solution:** Since the output of an ideal op amp is a dependent voltage source, only the resistances that come after the output it will come into play, which is why we saw only the divider at the output influence the resistance.

This highlights the benefit of an op amp in allowing circuits to present with a uncomplicated or choosable Thevenin equivalent resistance (e.g. a buffer, 0 resistance) so that designed circuit modules can be connected together with predictable effect.

9. **Homework Process and Study Group**

Who did you work with on this homework? List names and student ID’s. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

**Solution:**

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.