EECS 16A Designing Information Devices and Systems I
Spring 2020 Homework 8

This homework is due March 20, 2020, at 23:59.
Self-grades are due March 23, 2020, at 23:59.

Submission Format

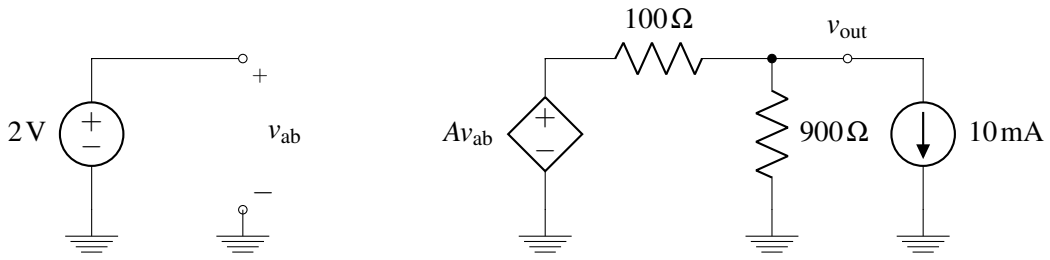
Your homework submission should consist of **one** file.

- `hw8.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. Superposition with a Dependent Source

Given $A = 5$, find the voltage v_{out} indicated in the circuit diagram below using superposition.



2. Super-Capacitors

In order to enable small devices for the "Internet of Things" (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are "super-capacitors" - the devices generally behave just like a "normal" capacitor but have been engineered to have extremely high values of capacitance relative to other devices that fit in to the same physical volume. They can function as a power supply for low power applications such as IoT devices and have the advantage that they can be charged and discharged many times without losing maximum charge capacity. That property makes super-capacitors suitable to store energy from intermittent power sources such as those from energy harvesting. Suppose you are tasked with designing a power supply with a super-capacitor in an IoT device.

(a) Assuming that your electronic device (load) can be modeled as a constant current source with a value of i_{load}, draw circuit models for your device using super-capacitors as the power supply with the following configurations:

- Config 1: a single super-capacitor as the power supply
- Config 2: two super-capacitors stacked in series as the power supply
- Config 3: two super-capacitors connected in parallel as the power supply

(b) If each super-capacitor is charged to an initial voltage v_{init} and has a capacitance of C_{sc}, for each of the three configurations above, write an expression for the voltage supplied to your electronic device as a function of time after the device has been activated (i.e. connected to the super-capacitor(s)).

(c) Now let's assume that your electronic device requires some minimum voltage v_{min} in order to function properly. For each of the three super-capacitor configurations, write an expression for the lifetime of the device.

(d) Assume that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor. You consider the two following configurations:

- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel

When is Config 3 (parallel) better than Config 2 (series)? Your answer should involve conditions on v_{init} and v_{min}.

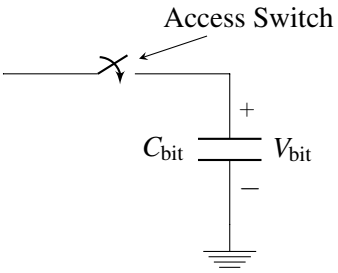
(e) Calculate the amount of energy delivered by the super-capacitors in Config 3 (parallel) over the device's lifetime.

3. Dynamic Random Access Memory (DRAM)

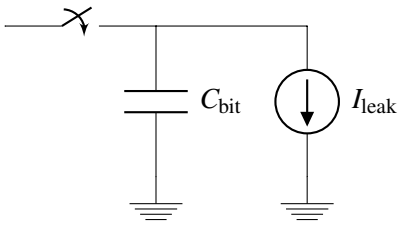
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location.

Single DRAM Bit Cell



In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, which we will model as a leakage to ground. The figure below shows a model of this leakage:



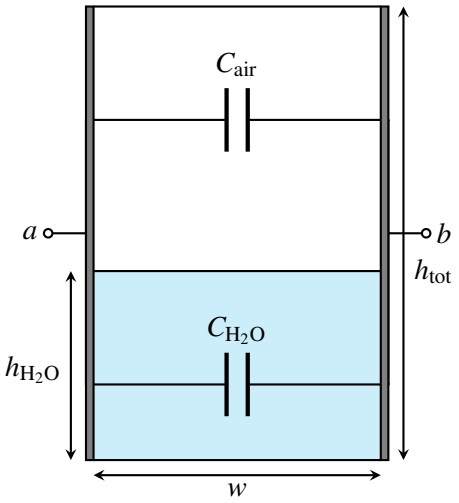
Fun Fact: This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 28\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.9\,\text{V}$ in order for the circuits outside of the column to properly read the bit stored in the cell as a "1."

What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

4. It's finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com's imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a rectangular tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.

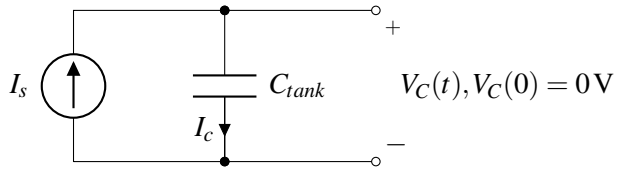


The width and length of the tank are both w (i.e., the base is square) and the height of the tank is h_{tot}.

(a) What is the capacitance between terminals a and b when the tank is full? What about when it is empty? *Note:* the permittivity of air is ε, and the permittivity of rainwater is 81ε.

(b) Suppose the height of the water in the tank is h_{H_2O}. Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance C_{tank}.

(c) After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:



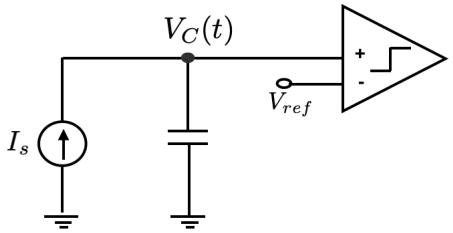
In this circuit, C_{tank} is the total tank capacitance that you calculated earlier. I_s is a known current supplied by a current source.

The suggestion is to measure V_C for a brief interval of time, and then use the difference to determine C_{tank}.

Determine $V_C(t)$, where t is the number of seconds elapsed since the start of the measurement. You should assume that before any measurements are taken, the voltage across C_{tank}, i.e. V_C, is initialized to 0 V, i.e. $V_C(0) = 0$.

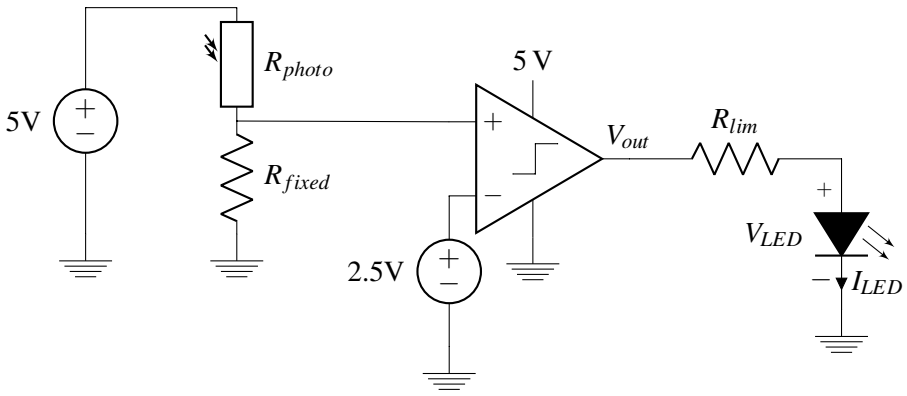
(d) Using the equation you derived for $V_C(t)$, describe how you can use this circuit to determine C_{tank} and $h_{\text{H}_2\text{O}}$.

(e) However, after spending some time thinking about different ways of measuring this capacitance you came up with a better idea. You decided to use the circuit proposed in part (c) along with a comparator, as show in the figure below. What you are basically interested in, is the time T_1 needed for V_c to reach V_{ref}. In order to measure time you use a timer. When voltage V_c becomes larger than V_{ref}, the comparator flips its value and you stop the timer. How would you measure in that case the value of the capacitance?



5. LED Alarm Circuit

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) "alarm" if the kitchen drawer is opened.



Note R_{photo} is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

V_{LED} indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is V_+, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of R_{photo} and R_{fixed}.

(b) We now want to choose a value for R_{fixed}. From the photoresistor's datasheet, we see the resistance in "light" conditions (i.e. drawer open) is $1\,k\Omega$. In "dark" conditions (i.e. drawer closed), the resistance is $10\,k\Omega$.

To ensure the comparator detects the light condition with more tolerance, we decide to design R_{fixed} so that V_+ is $3\,V$ under the "light" condition. Solve for the value of R_{fixed} to meet this specification.

(c) Write down V_{out} with any conditions in terms of V_+. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

(d) Using your answers to the previous parts, write down V_{out} with the conditions on its output in terms of R_{photo}. You can substitute the value of R_{fixed} you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

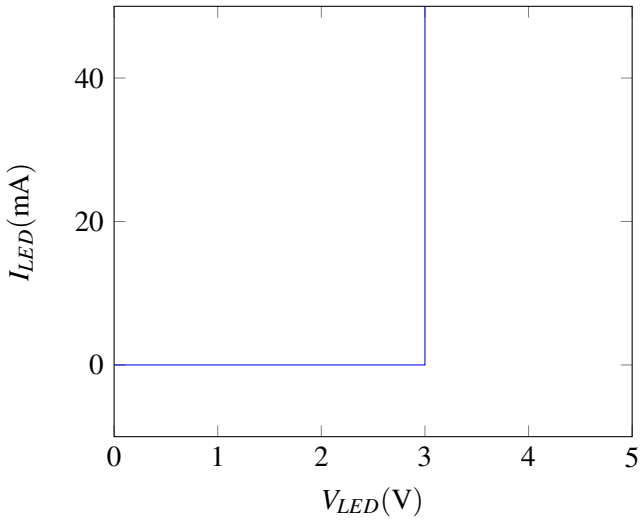
(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED's datasheet, the forward voltage, V_F is $3\,V$. Essentially, if V_{LED} is less than this voltage, the LED won't light up and I_{LED} will be $0\,A$.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:

i. If the voltage across the LED is less than $V_F = 3\,V$ or if $I_{LED} < 0\,A$, then the LED acts like an open circuit.

ii. If the voltage across the LED is $V_F = 3\,V$, then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).

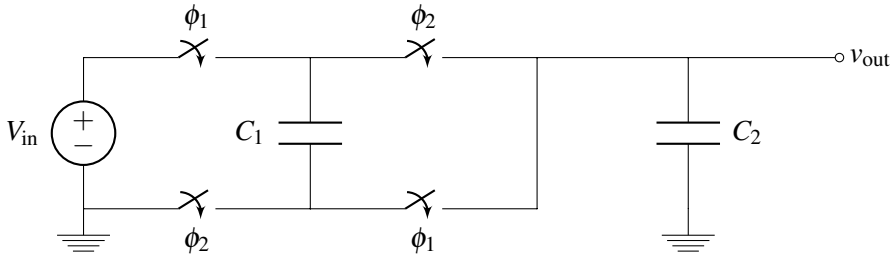


To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for I_{LED} is $20\,mA$.

Find the value of the current-limiting resistor, R_{lim}, such that when the photoresistor is in the "light" condition, $I_{LED} = 20\,mA$.

6. DC-DC Voltage Divider

One of the reasons for using AC voltages is that we can easily transform the voltage (step up or step down) using transformers. Unfortunately, such circuits do not work at DC and we need to come up with other ways of dividing DC voltages. We have learned about resistive dividers, but we found inefficiencies. An alternative circuit, a capacitive charge pump, is shown below. It relies on two switches that are activated in sequence. First, switch ϕ_1 is closed (during this period, ϕ_2 switches are open), and then ϕ_2 closes and ϕ_1 is opened. In practice, this is done periodically, but for this problem, we will analyze each phase separately. Note that V_{in} is a DC voltage.

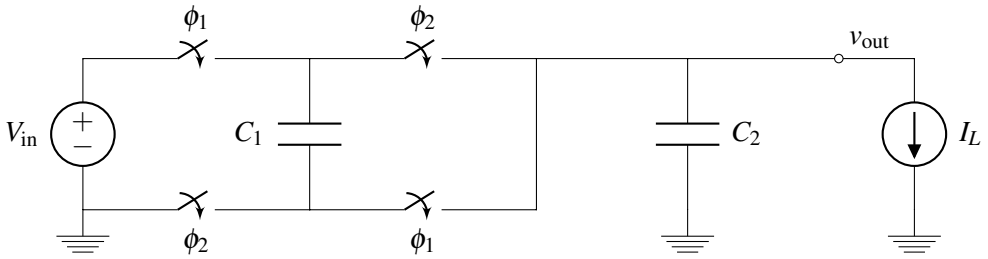


(a) During phase ϕ_1, calculate the voltage across and charge stored by each capacitor C_1 and C_2.

(b) During phase ϕ_2, calculate the output voltage v_{out} and show that it is a fraction of the input voltage V_{in}.

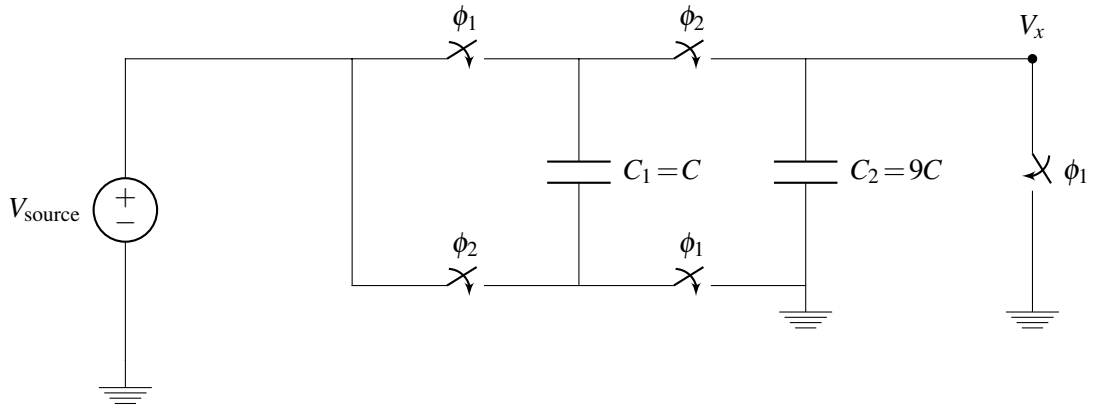
(c) For the special case of $C_1 = C_2$, calculate the output voltage and the efficiency of the system. To calculate the efficiency, calculate the energy stored in the capacitors at the end of phase ϕ_1 and ϕ_2.

(d) **PRACTICE:** Assume that this circuit is used with a load represented by the current source $I_L = 10\,\text{mA}$. Suppose that the cycle described above repeats periodically at a rate of 10 kHz, or 10,000 times per second, with each phase ϕ_1 and ϕ_2 lasting exactly 50% of each cycle. During phase ϕ_2, which lasts 50 µs, we want the output voltage to not decrease by more than 5 mV. Specify the capacitances of C_1 and C_2 to satisfy this constraint.



7. (PRACTICE) Charge Sharing

Consider the following circuit:



In the first phase, all of the switches labeled ϕ_1 will be closed and all switches labeled ϕ_2 will be open. In the second phase, all switches labeled ϕ_1 are opened and all switches labeled ϕ_2 are closed.

(a) Draw the polarity of the voltage (using $+$ and $-$ signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label $+$ or $-$; just remember to keep these consistent through phase 1 and 2!)

(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

(c) Find the voltage across and the charge on C_1 and C_2 in phase 1. Be sure to keep the polarities of the voltages the same!

(d) Now, in the second phase, find the voltage V_x.

(e) If the capacitor C_2 did not exist (i.e. had a capacitance of 0 F), what would the voltage V_x be?

8. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?